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consideration for allowance. No new matter has been added by any of the claim amendments.

## II. Claim Rejections Under 35 U.S.C. § 102

Claims 1-3 and 6-11 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,469,081 to Horita et al. (hereinafter, Horita). Applicant respectfully traverses the rejection and submits that the claims are allowable over the cited art for the following reasons.

Upon careful consideration and review of Horita, applicant respectfully submits that Horita does not disclose each and every element of the presently claimed invention and therefore does not anticipate the presently claimed invention. For example, Claim 1 recites an integrated circuit comprising a push-pull driving circuit having a first and second transistor being controllably independent. The Examiner states that Horita teaches "a first and second transistor (MP1, MP2) including control terminals (gate terminals) being controllably independent". Official Action, page 2. Applicant respectfully submits that Horita does not teach "a first and second transistor including control terminals being controllably independent". Referring to FIG. 2 of Horita, for example, inverters IN1 and IN2 are solely controlled by a single signal, signal LG, output from CMOS circuit 11. Therefore, inverters IN1 and IN2 of Horita are not controllably independent because of their connection to the output signal of CMOS circuit 11. Thus, applicant respectfully submits that Horita does not disclose a first and second transistor including control terminals being controllably independent. Therefore, applicant further urges that Horita does not disclose each and every element of the present invention and that the rejection of claim 1 under 35 U.S.C. §102(b) should be withdrawn.

Furthermore, Claim 1 recites a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second

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control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Applicant respectfully submits that Horita does not disclose a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal.

Referring to FIG. 2, for example, Horita teaches that CMOS circuit 11 can apply either a low level L or high level H to inverter IN1, IN2, and IN3 for causing transistor MP1 to be turned OFF and transistor MP2 to be turned ON or vice versa, respectively. Horita, column 7, lines 5-9 and 18-22. Horita does not disclose applying a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor. In fact, in Horita there is only one single control signal "LG" which is applied nearly simultaneously to the control terminals of the two transistors MP1 and MP2. The difference only results due to the signal propagation delay caused by the inverters IN1, IN2, and IN3. However, this delay caused by the signal propagation is not controllable in a way that the respective control terminals are being driven by a control signal being applied one after the other. Therefore, because Horita does not disclose applying a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, applicant submits that Horita does not disclose each and every element of the present invention and that the rejection of claim 1 under 35 U.S.C. §102(b) should be withdrawn.

Moreover, for example, terminal resistor R of Horita is provided to adjust the impedance of the signal path 13 to a predetermined value. Horita, column 6,

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lines 43-47. Terminal resistor R of Horita also affects the voltage level at output terminal OP1. For example, when a low level L is applied on signal line LG, the voltage level at output terminal OP1 equals voltage Vd minus the threshold voltage of transistor MP2 above the ground level, multiplied by the ratio of the resistance of the terminal resistor R to the sum of R and the ON-state resistor of transistor MP2. Horita, column 7, lines 28-33. Horita does not disclose a resistor coupled with the output of the integrated circuit and being of a pull-up or pull-down type, wherein the type of resistor determines whether a single positive or a single negative control pulse is applied on the output terminal. Rather, the output of transistors MP1 and MP2 is determined by the output logic signal LG of CMOS circuit 11. Horita, column 7, lines 10-16 and 34-36. Therefore, applicant further submits that Horita does not disclose each and every element of the present invention and that the rejection of claim 1 under 35 U.S.C. §102(b) should be withdrawn.

Claims 2 and 3 depend from Claim 1. Therefore, Claims 2 and 3 include the limitations of Claim 1. Thus, the comments presented above relating to amended Claim 1 apply equally to Claims 2 and 3. Furthermore, Claims 6 and 9 include limitations similar to those discussed above with regard to Claim 1. Claims 7 and 8 depend from Claim 6, and Claims 10 and 11 depend from Claim 9. Thus, the comments presented above relating to Claim 1 apply equally to Claims 6-11.

For the reasons provided above, applicant submits that Horita does not disclose each and every element of Claims 1-3 and 6-11. Therefore, applicant respectfully submits that the rejection of Claims 1-3 and 6-11 under 35 U.S.C. §102(b) should be withdrawn.

### III. Claim Rejections Under 35 U.S.C. § 103

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Horita in view of U.S. Patent No. 6,160,417 to Taguchi (hereinafter, Taguchi). This rejection is also respectfully traversed.

Regarding Claim 4, the Examiner states that Horita teaches all the claimed features of Claim 4 except that the first transistor is a P-channel MOS transistor and the second transistor is a N-channel MOS transistor. Official Action, page 4. The Examiner contends that Taguchi teaches the limitations not taught by Horita and that it would have been obvious to one of ordinary skill in the art to combine the teachings of Taguchi and Horita to arrive at the claimed invention. Official Action, page 4.

Regarding Claim 5, the Examiner states: "Taguchi further teaches in Fig. 3, the circuit as claimed in claim 4, wherein the first transistor (13) and the second transistor (14) form a CMOS inverter (12) with independent control gate connections (separate gate electrodes)". Official Action, page 5. Further, the Examiner contends that it would have been obvious to one of ordinary skill in the art to combine the teachings of Taguchi and Horita to arrive at Claim 5.

Claims 4 and 5 depend from Claim 1. As stated above, Claim 1 recites a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Summarily, neither Horita nor Taguchi, alone or in combination, discloses or suggests a single resistor being externally coupled with the output terminal of the integrated circuit and being of a pull-up or pull-down type, wherein the type of the resistor determines, by application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor, whether a single positive or a single negative control pulse being asynchronous to the applied control pulse and of the same duration is applied on the output terminal. Therefore, the combination proposed by the Examiner

does not offer a reasonable chance of success in combining the cited references.

As stated above, Horita does not disclose the above limitations of amended Claim 1. Taguchi fails to overcome the significant shortcomings of Horita. Taguchi is directed to a system for transmitting a small-amplitude signal between a microprocessor 5 and a SDRAM 20 via a bus line 15. Taguchi, column 1, lines 44-48. The system includes a push-pull-type output circuit 12 having a p-channel MOS transistor 13 functioning as a pull-up element and an n-channel MOS transistor 14 functioning as a push-down element. Taguchi, column 1, line 66, to column 2, line 2. As shown in Figure 3, transistors 13 and 14 are coupled in series between a line 26, which supplies VCC power, and a line 27, which supplies VSS power. Taguchi, column 2, lines 41-44. Microprocessor 5 includes an output terminal 6 connected to the coupling node of transistors 13 and 14 for connection to bus line 15. Taguchi, Figure 3. Microprocessor 5 can transmit a low signal to SDRAM 20 by turning transistor 13 off and transistor 14 on. Taguchi, column 2, lines 22-27. Further, microprocessor 5 can transmit a high signal to SDRAM 20 by turning transistor 13 on and transistor 14 off. Taguchi, column 2, lines 27-29. Summarily, the system of Taguchi can transmit either a high or low signal on bus line 15 depending on the signal input into transistors 13 and 14.

In contrast, the present invention, as claimed in amended Claim 1, applies only a single pulse on the output terminal in response to receiving both a positive and negative input pulse. The single input pulse is positive or negative depending on whether a single resistor, connected the output terminal, is of a pull-up or pull-down type. Thus, the output and input signals for the Taguchi system and the circuit of the presently claimed invention differ completely with regard to input and output. Therefore, applicant respectfully submits that Taguchi does not teach or suggest each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. Additionally, Taguchi offers no suggestion to modify the system

disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

Moreover, the resistors of the presently claimed invention provide an entirely different function than the resistors of the Taguchi system. Regarding Taguchi, the disclosed system includes termination resistors 28, 29, 30, and 31. Taguchi, column 2, lines 45-50. Taguchi discloses that resistors 28, 29, 30, and 31 are set approximately equal to 50 or 100 ohms. Taguchi, column 2, lines 46, 47, and 51-54. Resistors 28 and 29 and resistors 30 and 31 are connected in series across supply voltages VCC and VSS. Resistors 28, 29, 30, and 31 appear to perform the function of stabilizing the signal differences between lines 15, 26, and 27. In contrast, the single resistor recited in Claim 1 of the present application can be selected to be either a pull-up or pull-down type for determining whether a single positive or a single negative control pulse is applied on the output terminal. The single positive or single negative control pulse is applied on the output terminal in response to the application of a first control pulse on the control terminal of the second transistor and then a second control pulse on the control terminal of the first transistor. Thus, Taguchi does not teach each and every limitation of the presently claimed invention and, thus, cannot anticipate the presently claimed invention. For these reasons, it is respectfully submitted that the rejection of amended independent Claim 1 and dependent Claims 4 and 5 should now be withdrawn. Additionally, Taguchi offers no suggestion to modify the system disclosed therein to arrive at the presently claimed invention and, consequently, the combination proposed by the Examiner does not offer a reasonable chance of success in combining the cited references.

As stated above, Claims 4 and 5 depend from claim 1. Therefore, the comments presented above relating to Claim 1 apply equally to Claims 4 and 5.

Applicant respectfully submits that the teachings of Horita and Taguchi cannot be combined to either teach or suggest each and every element of the

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present invention. Therefore, Claims 4 and 5 are believed to be patentably distinguished over the cited references. Applicant respectfully requests that the rejections of Claims 4 and 5 under 35 U.S.C. §103(a) be withdrawn and the claims allowed at this time.

#### IV. New Claims

Claims 12-14 have been added. Claims 12-14 depend from Claims 1, 6, and 9. No new matter has been added by any of the new claims. Support for new claims 12-14 can be found, for example, at page 4, lines 9-15 of the present application. Applicant respectfully requests notification of the allowance of new Claims 12-14 since Claims 12-14 depend from Claims 1, 6, and 9 which are believed to be allowable for the reasons set forth above.

#### CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and such action is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

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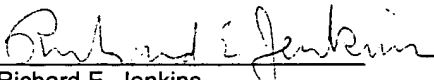
The Commissioner is hereby authorized to charge any fees associated with the filing of this correspondence to Deposit Account Number 50-0426.

Respectfully submitted,

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